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(54) COMPUTER SYSTEM

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SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

BE IT KNOWN that I, RUDOLF KOBER, a citizen of Germany, residing at Rattenberger Strasse 30, 8000 Muenchen 70, Germany, have invented certain new and useful improvements in

"A COMPUTER SYSTEM"

and I do hereby declare that the following is a full, clear and exact description of the same, reference being had to the accompanying sheets of drawing and to the numerals of reference marked thereon which form a part of this specification.

ABSTRACT OF THE DISCLOSURE

A computer system includes a number of individual computers which can be coupled to a control computer by way of a system bus which comprises at least two bus systems, in particular an address and control bus and at least one data bus. The system bus is divided into sections by one or more bus switches and each bus switch operates such that the two bus systems can be interrupted under its control, its flow-through direction can be separately switched over for each of the bus systems and it can be directly addressed by a control computer and at least one data exchange computer is connected to the system bus at various points.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a computer system wherein a number of individual computers can be coupled to a control computer by way of a system bus which comprises at least two bus systems including an address and control bus and at least one data bus.

Description of the Prior Art

A computer system of the type generally described above is known from the German published application 25 46 202. In this computer system the control computer distributes the data by consecutively supplying the operational result of each individual computer to the system bus and recording this result in the remaining individual computers, irrespectively of how many individual computers utilize the result. Therefore, the number of exchange cycles required for the total data exchange corresponds to the number of results which must be distributed to the individual computers.

The degree of efficiency of computer systems of the type mentioned above is greatly dependent upon the duration of the information exchange between the individual computers. It is therefore desirable to achieve as short as possible an exchange interval.

Many problems which must be processed involve limited vicinity coupling, i.e. data only requires to be exchanged between adjacent elementary functions. In computer systems of the type described above, this means that an exchange is only required between

those individual computers which are arranged at a limited distance from one another. Limited vicinity coupling between individual computers in a computer system is known from field computers. In this connection, one may refer to G.H.Barnes, R.M.Brown, M. Kato, D.J.Kuck, D.L.Slotnik, R.A. Stokes: "The ILLIAC IV Computer", IEEE Transactions on Computers, Vol. C-17, No. 8, August 1968, wherein the individual computers are permanently coupled to one another, e.g. each individual computer is coupled to four neighboring computers. This rigid coupling is only advantageous, however, in the case of a few problems; in the case of problems in which the coupling does not conform with the computer structure such as occurs, for example, in the case of couplings of higher order or irregular coupling, the rigidity complicates and slows down the data exchange to a considerable extent giving rise to long exchange durations.

SUMMARY OF THE INVENTION

The primary object of the present invention is to provide a computer system of the type mentioned above wherein the limited vicinity coupling can be exploited in order to achieve a reduction in the exchange phase.

This object is achieved in that the system bus is divided into sections by means of one or more bus switches and that each bus switch possesses the following characteristics:

(a) the two bus systems can be interrupted under its control;

(b) its flow-through direction can be separately switched over for each of the bus systems; and

(c) it can be directly addressed by the control computer, and that at least one data exchange computer is connected to the system bus at different points.

In the case of problems involving heavy or irregular coupling, this computer system allows all of the bus switches to be closed and the results to be exchanged between all of the individual computers. In the case of problems involving limited vicinity coupling, by opening bus switches it is possible to divide the system into a plurality of sections within which the data exchange can take place simultaneously and independently in each case under the control of a data exchange computer.

As a result of this parallel exchange of data, the exchange phase can be considerably shortened in the case of many problems.

An advantageous embodiment of the invention is constructed such that a bus switch is arranged between two adjacent points at which an individual computer can be connected to the system bus.

Another advantageous embodiment of the invention provides that a data exchange computer is connected to every second connection point.

An advantageous further feature of the invention is that in a system one or more groups which each comprise two or more adjacent bus switches can be bridged by a further bus switch, and that each further bus switch possesses the following characteristics:

(a) its flow-through direction can be switched over;

(b) the switch is enabled when all the switches within the group which it bridges are enabled and simultaneously interrupts a switch within the group located at one end; and

(c) it interrupts when at least one of the other switches within the group is interrupted.

A computer system constructed in accordance with the present invention is advantageously further developed in such a manner that a multi-stage bridging system is formed so that in each stage, with the exception of the highest stage, one or more than one group, each of which comprises two or more further bus switches, can be bridged by a further bus switch of the next higher stage, where the lowest stage comprises the further bus switches by which the bus switches on the system bus can be bridged, and that each further bus switch which bridges a group of further bus switches possesses the following characteristics:

(a) its flow-through direction can be switched over;

(b) the switch is enabled when all of the switches within the group which it bridges are enabled and simultaneously interrupts a switch within the group located at one end; and

(c) it interrupts when at least one of the other switches within the group is interrupted.

According to a broad aspect of the invention, there is provided, in a computer system of the type in which a plurality of individual computers are operatively connected to a control computer by way of at least two bus systems including an address and control bus and at least one data bus, the improvement therein comprising at least one bus switch connected in and operable to interrupt said bus systems into sections, including means for controlling the flow-through direction separately for each of the bus systems, at least one data exchange computer and means for connecting the data exchange computer into the bus system at a point along the bus systems.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects, features and advantages of the invention, its organization, construction and mode of operation will be best understood from the following detailed description, taken in conjunction with the accompanying drawings, on which:

FIG. 1 is a block diagram of the construction of the computer system;

FIG. 2 is a block diagram of a two-stage bridging system;

FIG. 3 is a two-dimensional grid network;

FIG. 4 illustrates a linear diagram;

FIG. 5 is a block diagram which illustrates an exemplary embodiment of a bus switch and of a further bus switch;

FIG. 6 is a block diagram illustration of the construction of a two-path bus driver;

FIG. 7 is a schematic logic diagram of the construction of the control logic of the bus switch illustrated in FIG. 5;

FIG. 8 is a block diagram illustration of the construction of the selection logic for the bus switch illustrated in FIG. 5;

FIG. 9 is a logic circuit diagram of the construction of the release logic for the bus switch illustrated in FIG. 5;

FIG. 10 is a block system diagram illustrating the design of a bridging of a group of switches and further bus switches by a further bus switch;

FIG. 11 illustrates two data flow diagrams for a bridging operation;

FIG. 12 is a schematic block diagram which illustrates an exemplary embodiment of the interconnection of the adjacent bus switches;

FIG. 13 is a block diagram illustrating an exemplary embodiment of the principle of directional switch-over; and

FIG. 14 is a data flow diagram relating to the two-stage bridging system illustrated in FIG. 2.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. 1, a plurality of individual computers M_1--M_6 are connected to a system bus 1 at respective points m_1--m_6. Between two adjacent connection points m_i and m_{i+1}, a bus switch S_i is arranged in the system bus. There are, accordingly, five bus switches S_1--S_5 available in this particular system. The bus switches serve to divide the system bus into sections a_1--a_6. At the points m_2, m_4 and m_6 of the system bus, a data exchange computer ATR_1, ATR_2 and ATR_3 is respectively connected. On the left-hand side of the system bus a control computer STR is connected. The system can be imagined to continue on the right-hand side. Preferably, a

computer system of this type is constructed by means of microprocessor modules.

FIG. 2 schematically illustrates a two-stage bridging system. The bus switches S_6--S_{20} are arranged on a system bus 2. The bus switches S_9--S_{11} can be bridged by a further bus switch S_{21}, the bus switches S_{12}--S_{14} can be bridged by a further bus switch S_{22}, and the bus switches S_{15}--S_{17} can be bridged by a further bus switch S_{23}.

Here the further bus switches S_{21}--S_{23} form the first stage of the bridging system. These bus switches, in turn, can be bridged by a further bus switch S_{24} which forms the second stage of the bridging system. Each of the further bus switches must be able to fulfill the following functions:

its flow-through direction must be able to be switched over;

it must be enabled when all of the bus switches or further bus switches in the next lower stage which it serves to bridge are themselves enabled and must simultaneously interrupt a switch within this group located at one end; and

it must interrupt when at least one of the other switches within this group is interrupted.

Before a specific example of a computer system of the type illustrated in FIGS. 1 or 2 will be discussed in detail, reference will be taken to FIGS. 3 and 4 to illustrate how, in the described computer structure, the exchange width can be matched to the coupling width of

the problem to be handled. Here, the influence of the coupling method upon the duration of the data exchange will be investigated in the form of an example. The example considered will be a two-dimensional problem structure such as illustrated in FIG. 3. Structures of this kind occur in the solution of partial differential equations in accordance with a method of finite differences which is used, for example, in field calculations or in weather forecasting. Here, data exchange is only required between directly adjacent grid network points. In FIG. 3 this has been emphasized in the example of the network point i, which exchanges data only with its four closest neighbors $i - 1$, $i - n$, $i + 1$ and $i + n$. This problem can be represented in the given linear computer structure, for example, as illustrated in FIGS. 1 or 2, in which each individual computer deals with one grid network point, in such a manner that data exchange is only required within a specific bandwidth. The individual computer which is assigned to the grid network point i must distribute its results between the individual computers assigned to the points $i - n$, $i - 1$, $i + 1$ and $i + n$. Therefore, the band width amounts to $2n + 1$. These facts projected onto a single dimension are illustrated in FIG. 4.

The proposed computer system can be advantageously adapted to this problem by dividing the system bus into sections of the length $2n + 1$. The bus switches effect this division. The result of the particular middle individual computer is distributed within these sections. As a next stage, the sections of the system bus are displaced by one bus switch and the results of the individual computers now located in

the center of the sections are distributed, and so on. As exchange takes place simultaneously in all sections, only two n + 1 exchange steps are required in order to distribute n^2 results. As a result, the data exchange phase is reduced by a factor which is equal to the ratio of the number of grid network points/bandwidth. In the case of a two-dimensional problem where n = 100, which corresponds to a number of grid points of 10^4 and a bandwidth of 201, the number of exchange steps is reduced by approximately 1/50 of the number of grid network points. Here, it must be expressly pointed out that the proposed computer system is not limited to this example, but can be advantageously adapted to other problem structures. The basis for this resides in the aforementioned characteristics which the bus switches must possess.

Referring to FIG. 5, a particularly advantageous embodiment of a bus switch is illustrated. This embodiment is designed to be such that it can be used simultaneously as a further bus switch. According to FIG. 5, the bus switch comprises a selection logic SSL, a release logic SEL, two two-path bus drivers BD1 and BD2, connected to the system bus, with associated control logics BC1 and BC2, where the bus driver BD1 is connected into the data bus and the bus driver BD2 is connected into the address bus, and further comprises an operating mode transfer switch S. With the aid of the operating mode transfer switch S it is possible to switch between two operating modes, in one of which, which here is referenced A, the bus switch state is determined by the release logic SEL, and therefore is addressed and controlled by the control computer. In the other operating mode,

which here has been referenced B, the operating state is established via an ENABLE input which can be connected to a ENABLED-output of another bus switch constructed in a similar manner, as a result of which the bus switch can adopt the operating state of the other. When the bus switch is employed as a further bus switch in a stage of a one-stage or multi-stage bridging system, the ENABLED outputs of the bridged switches in the next lower stage are connected by way of an AND gate to the ENABLE input of this further bus switch, as a result of which the characteristics mentioned above are achieved in the latter, namely, the switch, the switch is enabled when all of the switches within the group which it bridges are enabled and simultaneously interrupts a switch within the group located at one end, and it interrupts when at least one of the other switches within the group is interrupted. Between the ENABLED output and the operating mode transfer switch S there is also connected a driver 50 having an open collector output, which facilitates a wired AND logic link between the ENABLED outputs of a plurality of bus switches.

FIG. 6 illustrates the construction of the two bidirectional bus drivers BD1 and BD2 which are of identical construction. This is a bus driver for bit-parallel transmission of a byte which is composed of two four-bit-parallel two-path bus drivers SAB 8216 (see detailed description in Mikro-processor-Bausteine "Datenbuch" 1976/77, System SAB 8080 by Siemens AG, Bereich Bauelemente, Balanstrasse 73, 8000 Muenchen 80). Here, and in the following, the inputs and outputs of the modules will be provided with the references given in the above-

mentioned publication. By way of the inputs $\overline{CS}$ of the two modules which are connected to a common input $\overline{cs}$, the bus driver can be blocked. The direction of the data flow is determined by way of the inputs $\overline{DIEN}$ which are linked to a common input $\overline{dien}$ of the bus driver. Further details are provided in the above-mentioned publication. The terminals DI, DO and DB act as substitutes for the inputs DI_0--DI_3, DO_0--DO_3 and DB_0--DB_3 given therein.

FIG. 7 is a detailed illustration of the construction of the control logic BC1 and BC2. The module 7408 is suitable for the three AND gates AD1, AD2 and AD3 each of which has two inputs, the module 7427 is suitable for the NOR gates, the module 7404 is suitable for the inverters 85 and 86, and the modules 7422 having an open collector is suitable for the NAND gate 87 which has three inputs, all produced by Siemens AG (see "Digitale Schaltungen", Datenbuch 1976/77 of Siemens AG, published by Bereich Bauelemente, Vertrieb, 8000 Muenchen 80, Balanstrasse 73). The direction of the input DIR CTRL 1 and DIR CTRL 2 can be determined by way of the input DIR CTRL IN1 to which it is connected. This input is connected, on the one hand, by way of the inverter 85 to an input of both the NAND gate 87 and the AND gate 81 and, on the other hand, is directly connected to an input of the AND gate 83. In addition, a direct connection exists between the aforementioned input and the output 702 which is connected to the input $\overline{dien}$ of the associated two-path bus driver. The input enable 1 and enable 2 is connected, on the one hand, to the output 53 of the operating mode transfer switch S and, on the other hand, to the

second input of the AND gate 83 and to a second input of the gate 87 and to an input of the NOR gate 84. The main function of the input enable 1 is, by way of the output 701 which must be connected on the one hand to the output of the NOR gate 84 and on the other hand to the input $\overline{cs}$ of the two-path bus driver BD1 and BD2, to block or release the latter. When the relevant bus driver is released, via the input enable 1 or enable 2 of the control logic, the directional information can be forwarded to the next bus switch. This information is input into the bus switch via the inputs DIR CTRL IN1 and DIR CTRL IN2 (see FIG. 5). An input DISL of the control logic is connected to the second input of the AND gate 81, whereas the input DISR1 and DISR2 is connected to an input of the AND gate 82. The output of each of these AND gates is connected to a second and third input of the NOR gate 84. The one input of the AND gate 82 is connected by way of an inverter 86 to the third input of a NAND gate 87, and the second input of the AND gate 82 is connected to the first input of the NAND gate 87. The bus drivers BD1 and BD2 can be selectively blocked for a right-hand or left-hand data flow direction via the inputs DISR1 and DISR2. The output of the AND gate 83 forms the output DISR OUT1 and DISR OUT2 of the bus switch. The latter output is required in a one-stage or multi-stage bridging system. The output of the NOR gate 87 forms the output DIR CTRL OUT1 and DIR CTRL OUT2 of the bus switch.

FIG. 8 is a detailed illustration of the switch selection logic SSL. The switch selection logic comprises two four-bit comparators 81 and 82 arranged next to one another, such as the module 7485 in "Digitale Schaltungen", supra, Pages 122 and 123. The inputs 2 ($A < B$), 3 ($A = B$) and 4 ($A > B$) of the comparator 82, as referenced in the above-mentioned publication, are connected in parallel with the corresponding outputs 7 ($A < B$), 6 ($A = B$) and 5 ($A > B$) of the comparator 81. The four-bit terminals A and B are identical to the terminals A_0--A_3 and B_0--B_3 in the publication. The terminals A of the two comparators 81 and 82 together form a byte terminal which must be connected to the address bus. The four-bit terminals B of the two comparators are connected in parallel to an eight-times coder switch having a pull-up resistor. The input 3 ($A = B$) of the comparator 81 is connected via a resistor 84 to the supply voltage which corresponds to the binary logic value "1", whereas the output 6 ($A = B$) of the comparator 82 is connected to the "selected" input of the release logic SEL. With the coder switch 83 schematically illustrated in FIG. 8, the bus switch can be provided with a fixed switch number. If the address input via the inputs A agrees with the switch number, the output 6 ($A = B$) is connected to a logic "1".

FIG. 9 illustrates the release logic SEL in detail. This circuit contains four OR gates 91--94 each having two inputs, two AND gates 95 and 96 each having three inputs, a D-flip-flop 97 and an inverter 98. The "selected" input is connected by way of the

inverter 98 to an output of the OR gate 91. The output of the OR gate 91 is connected, on the one hand, to an input of the AND gate 95 and to an input of the AND gate 96. The output of the AND gate 95 is connected to the input D, and the output of the AND gate 96 is connected to the input T of the D-flip-flop 97 (for example the module 7474 in the aforementioned publication "Digitale Schaltungen", Pages 190 and 191, the inputs and outputs referenced as therein). The input R of the flip-flop 97 is connected to the $\overline{\text{RESET}}$ input of the bus switch. The input S of the flip-flop is continuously connected to a logic "1". The output Q of the flip-flop 97 is connected to an input of the OR gate 94, to the outputs EN RIGHT OUT and EN LEFT OUT of the bus switch (see FIG. 5). The output of the OR gate 94 forms the enabled output of the release logic which is connected to the input 51 of the operating mode transfer switch S whose other input 52 is connected to the input ENABLE of the bus switch. The input $\overline{\text{SHIFT RIGHT}}$ of the bus switch is connected, on the one hand, to a second input of the AND gate 96 and to an input of the OR gate 93. Similarly, the input $\overline{\text{SHIFT LEFT}}$ of the bus switch is connected to the third input of the AND gate 96 and to an input of the OR gate 92. The input $\overline{\text{SELECTION MODE}}$ is connected to the second input of the OR gate 94, whereas the input $\overline{\text{SELECT STB}}$ is connected to the second input of the OR gate 91, and the input EN LEFT IN is connected to the second input of the OR gate 92. The output of the OR gate 92 is connected to a second input and the output of the OR gate 93 to the third input of the AND gate 95. The D-flip-flop 97 which serves as a marker flip-flop can be set by three different

signals:

If the bus switch is selected (selected "1"), with a $\overline{\text{SELECT STB}}$ pulse marking flip-flop is set at a logic "0", i.e. the output Q is connected to "0";
With a $\overline{\text{SHIFT LEFT}}$ pulse, the flip-flop is loaded with the state of the input EN LEFT IN; and
With a $\overline{\text{SHIFT RIGHT}}$ pulse, is loaded with the state of the input SHIFT RIGHT IN which is connected to the second input of the OR gate 93.

The advantageous circuit comprising SHIFT LEFT and SHIFT RIGHT which has been described is intended to facilitate a simple shift of bus sections which have already been divided by connecting a $\overline{\text{SHIFT LEFT}}$ or $\overline{\text{SHIFT RIGHT}}$ pulse, as a result of which the computer system can be particularly advantageously employed for problem structures such as described in FIGS. 3 and 4.

When the $\overline{\text{SELECTION MODE}}$ input is connected to a logic "0" the relevant binary value present at the output Q of the flip-flop is connected to the enabled output. The bus switch now interrupts when the enabled output carries "0". Otherwise it is open. If the $\overline{\text{SELECTION MODE}}$ input is connected to a logic "1" enable likewise carries this value, which means that the bus switch is closed. In this manner it is possible to switch over between a system bus divided into sections and a through-going system bus without any loss of time. The marking flip-flop can be reset to the basic position Q = "1" by way of the $\overline{\text{RESET}}$ input. The function of the marking flip-flop is to

"mark" the bus switches which are to interrupt in the case of the "selection mode" operating mode. As described above, this marking can be carried out in three different ways. The bus switch remains closed, however, if a "1" is present at the $\overline{\text{SELECTION MODE}}$ input. As a result, items of information can be transmitted from the control computer to all of the computers, data exchange computers and bus switches provided in the system. As a result, the sequence of marking of the bus switches is arbitrary. If, on the other hand, the bus switch were to interrupt immediately, all the components located behind the switch would be unable to be approached by the control computer. It would therefore be necessary to first interrupt the more remote bus switches. If the input $\overline{\text{SELECTION MODE}}$ is connected to a "0", the system bus is interrupted at the marked points.

During a data exchange with a divided system bus, a temporary and short-term necessity can consist in gaining access from the control computer to all or a few of the more remote components, for example in order to modify the programs in the data exchange computers. For this purpose, the time saving transfer between divided and through-connected system bus configuration is provided which can be achieved in a very simple manner with the aid of the flip-flop.

FIG. 10 illustrates a bridging of four bus switches S_{101}--S_{104} by a further bus switch S_{201}. Each of the switches is constructed as illustrated in FIG. 5. The ENABLED outputs of the four bus switches are connected via a wired AND circuit to the ENABLE input of the

further bus switch and to the DISL input of the bus switch S_{101}. The outputs DISR1 OUT and DISR2 OUT of the further bus switch are connected to the corresponding inputs DISR1 and DISR2 of the bus switch S_{104}. In the case of all the other bus switches and the further bus switch, these inputs are connected to ground. Apart from the bus switch S_{101}, in the case of the further bus switch and all the other bus switches, the inputs DISL are likewise connected to ground. The inputs DIR CTRL1 and DIR CTRL2 are connected to the control computer via control lines DIR CTRL1+ 2. All the other inputs and outputs of the bus switches are likewise connected to the control computer via a control bus SWITCH CONTROL BUS. The mode of operation of this connection is such that when all the bus switches are released, and the further bus switch is likewise released, simultaneously, via the inputs DISL, the left-hand bus switch S_{101} is blocked in respect of the left-hand data flow direction and via the inputs DISR1 and DISR2 the right-hand bus switch S_{101} is blocked in respect of right-hand directions. (An exception is formed by the bridging of arms with data sources which will be described later in this description.) In this manner, the data paths 101 and 112 illustrated in FIG. 11 are formed.

The illustrated bridging can be used for any bridging stage. This means that the switches S_{101}--S_{104} can equally constitute further bus switches of the first or a higher stage of a bridging system. In this manner it is possible to construct any multi-stage bridging system.

In FIG. 12, a zone 120 framed in broken lines in FIG. 10 has been illustrated in full detail.

Here the inputs and outputs whose use is dependent upon the setting of the switch are marked with an asterisk. When the switch is used as a bus switch in a system without bridgings, all three inputs DISR1, DISR2 and DISL are connected to ground. With bridgings, the interconnection of the four upper outputs can be gathered from FIG. 10. The same applies when the switch S_{102} is a left-hand end switch and the switch S_{103} is a right-hand end switch. The wiring of the other inputs and outputs of the two switches, therefore the switches which are not marked with an asterisk, is obvious from FIG. 12.

FIG. 13 illustrates four bus switches S_{121}--S_{124} on a data bus 125 of a computer system. The directional transfer is to be explained on the basis of this drawing. Between two adjacent bus switches, an individual computer or data exchange computer is connected as the source Q_1--Q_3 of information to the data bus. The construction of the bus switches is as illustrated in FIG. 5, with the difference that the selection logic BC1 and BC2 is replaced by a simplified, extra logic in each case provided with a driver and a resistor. The function of this simplified logic is identical to that illustrated in FIG. 7, when the inputs DISR1 and DISR2, DISL, DIR CTRL IN 1 and DIR CTRL IN 2 are connected to a logic "0" and enable 1 and enable 2 are connected to "1". In FIG. 13 the input $\overline{\text{dien}}$ of the bus driver BD1 of each bus switch is connected to a

control line DIR CTRL. Between two adjacent connection points, a driver having an open collector output is arranged in the control line, and furthermore each of these sections can be connected by way of a resistor to the supply voltage. The drivers are provided with the references 131--134 and the resistors with the references 135--138. Each source has an output q_1, q_2 or q_3 which is connected to the control line DIR CTRL. This output is connected to a logic "0" when the source is transmitting, i.e. when the individual computer or exchange computer is emitting data. An arrangement which is of identical construction and which is provided with a control line to which sources are connected can be additionally provided for the inputs dien of the two-path bus driver BD2.

The arrangement illustrated in FIG. 13 realizes the principle of directional transfer. This is based upon the following considerations:

In each bus section, there is only one transmitting source for each bus system in each exchange cycle.

In the case of the control and address bus this can be the control computer or an exchange computer and in the case of the data bus can consist of a specific individual computer. This source transmits information to the remaining elements of the bus section; this means that the bus drivers must be connected in the direction leading away from the source.

The principle of directional transfer is identical for both bus systems; therefore, only the data bus system has been illustrated in FIG. 13. In FIG. 13 the bus driver direction is controlled via the control line DIR CTRL. If no source is transmitting, it is connected to a logic "1", which is effected by the resistors. As a result, the drivers are connected to the right-hand direction. If a source now wishes to transmit information, it connects a logic "0" to the associated section of the control line. This value is communicated to the drivers arranged on the left-hand of the source and consequently these drivers reverse their direction to the left. As a result, the source can emit its information in a radiating fashion.

In the case of bridged arms of a bridging system, the source must connect such control lines DIR CTRL of the further bus switches in the same way to a logic "0". In FIG. 14, the data flow in the case of sources within bridged sections of a bridging system corresponding to FIG. 2 has been represented by way of example. The items of information emitted from the source are forwarded to a bridged section of the next higher stage via the extreme right bus switch of the bridged section to which the source is connected. The same then applies to the forwarding from stage to stage. Therefore, in this case for each stage the extreme right bus driver of a section which receives information from the next lower stage is not blocked for the right-hand data flow direction, even when all the bus switches in this section are released. The output DISR OUT of the bridging bus switch is inactive because its data flow direction is toward the left.

Finally, the function of the data exchange computer will be described. When the system bus has been divided into sections, these sections represent independent computer systems and require a "central" computer which undertakes the distribution of the results within the independent section. In this case it must fulfill the two following functions:

(1) Switching of a data path upon which data is to be transmitted; and

(2) Transmission of data on this path.

This can be fundamentally effected by any suitably programmed computer. However, data exchange computers especially set up for this purpose have been proposed, as disclosed, for example, in the German patent application P 26 41 741.4, which computers are also highly suitable for the computer system described herein.

Although I have described my invention by reference to particular illustrative embodiments thereof, many changes and modifications of the invention may become apparent to those skilled in the art without departing from the spirit and scope of the invention. I therefore intend to include within the patent warranted hereon all such changes and modifications as may reasonably and properly be included within the scope of my contribution to the art.

I CLAIM:

1. In a computer system of the type in which a plurality of individual computers are operatively connected to a control computer by way of at least two bus systems including an address and control bus and at least one data bus, the improvement therein comprising

at least one bus switch connected in and operable to interrupt said bus systems into sections, including means for controlling the flow-through direction separately for each of the bus systems, at least one data exchange computer and means for connecting the data exchange computer into the bus system at a ~~respective~~ point along the bus systems.

B

2. The improved computer system of claim 1, wherein each of the individual computers is connected to respective points along the bus systems, and comprising a respective bus switch connected between adjacent ones of said points.

3. The improved computer system of claim 2, comprising a separate data exchange computer operatively connected at each of said points.

4. The improved computer system of claim 3, comprising a bus switch group including
at least one further bus switch bridging at least two adjacent bus switches comprising means for controlling the flow-through direction, means for enabling the further bus switch when all the bus switches within the group are enabled and simultaneously interrupting the bus switch within the group at one end of the selected section, and means for interrupting said further bus switch when at least one bus switch within the group is interrupted.

FETHERSTONHAUGH & CO.
OTTAWA, CANADA

PATENT AGENTS

7-1

Fig.1

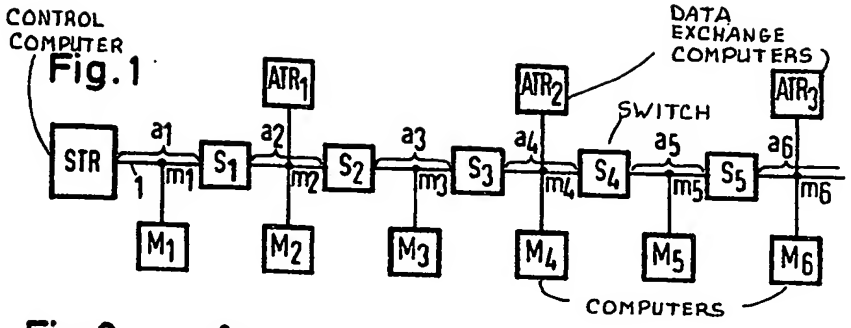

Fig.2

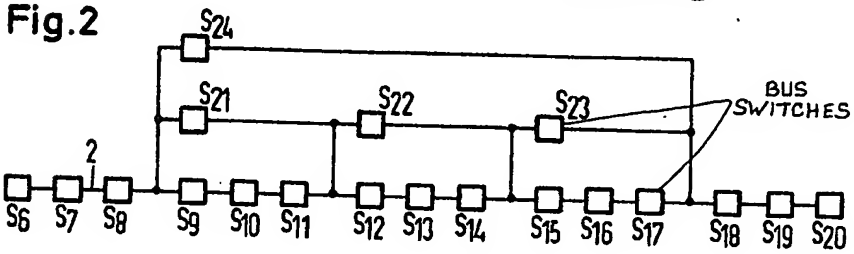

Fig.3

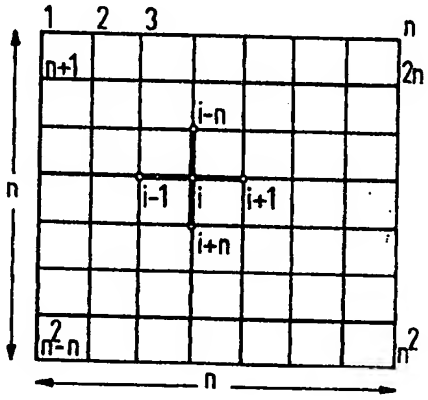

Fig.4

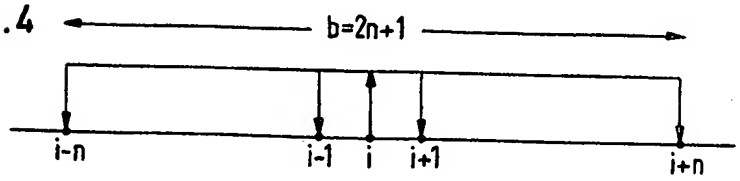

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Fig. 5

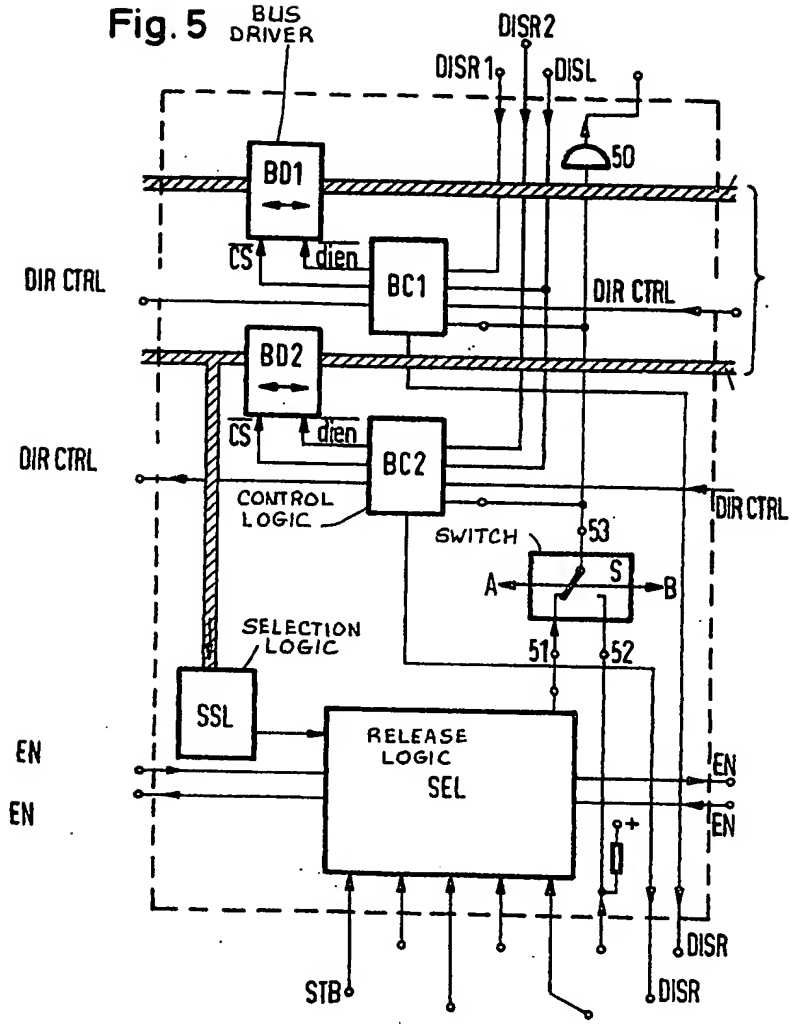

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Fig.6

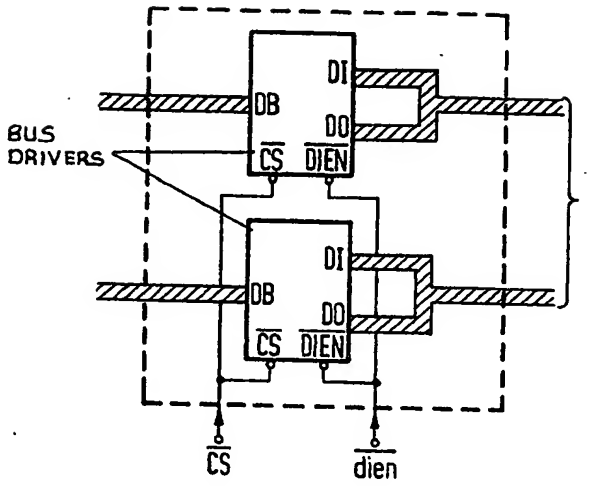

Fig.7

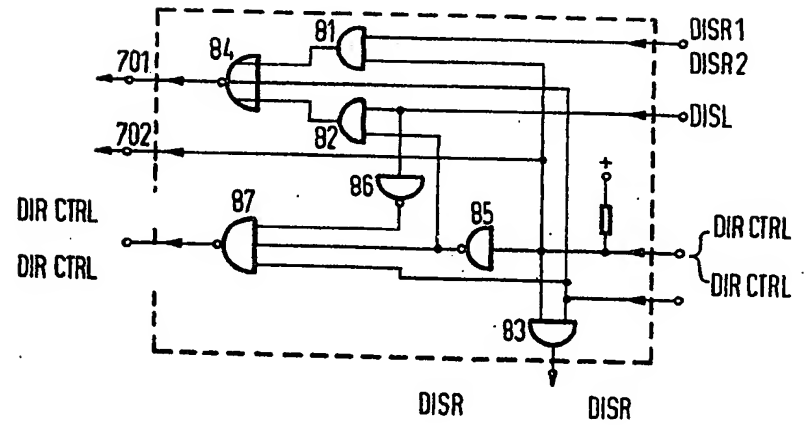

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Fig. 8

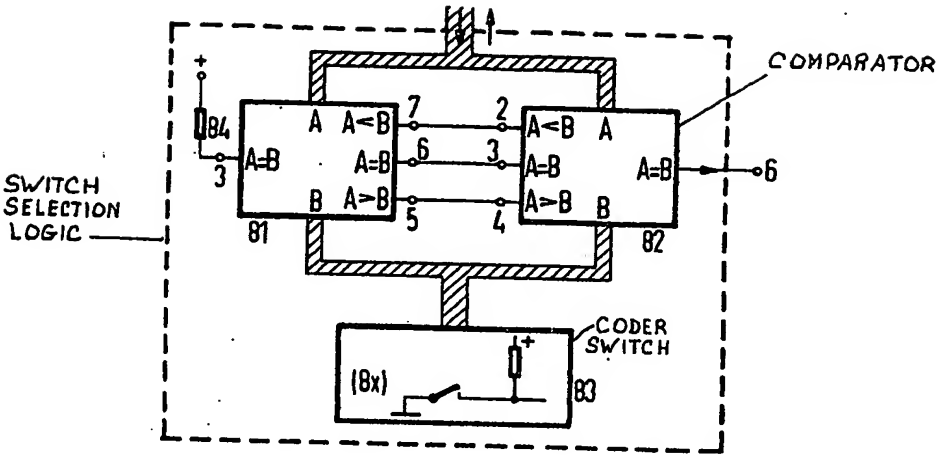

Fig. 9

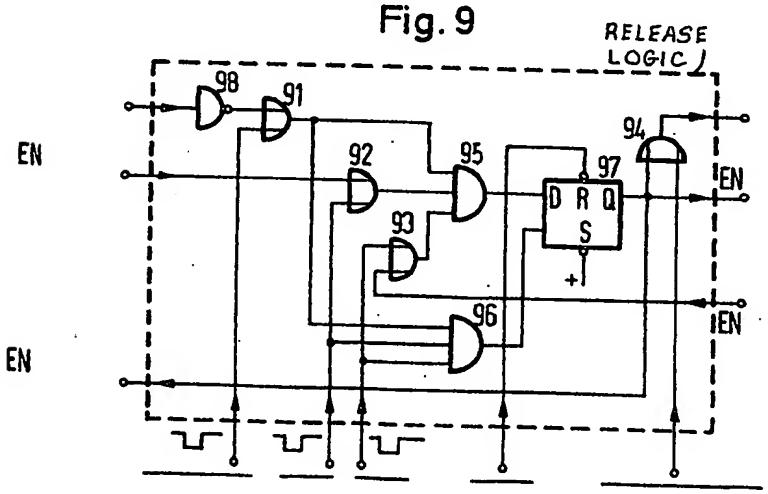

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Fig. 10

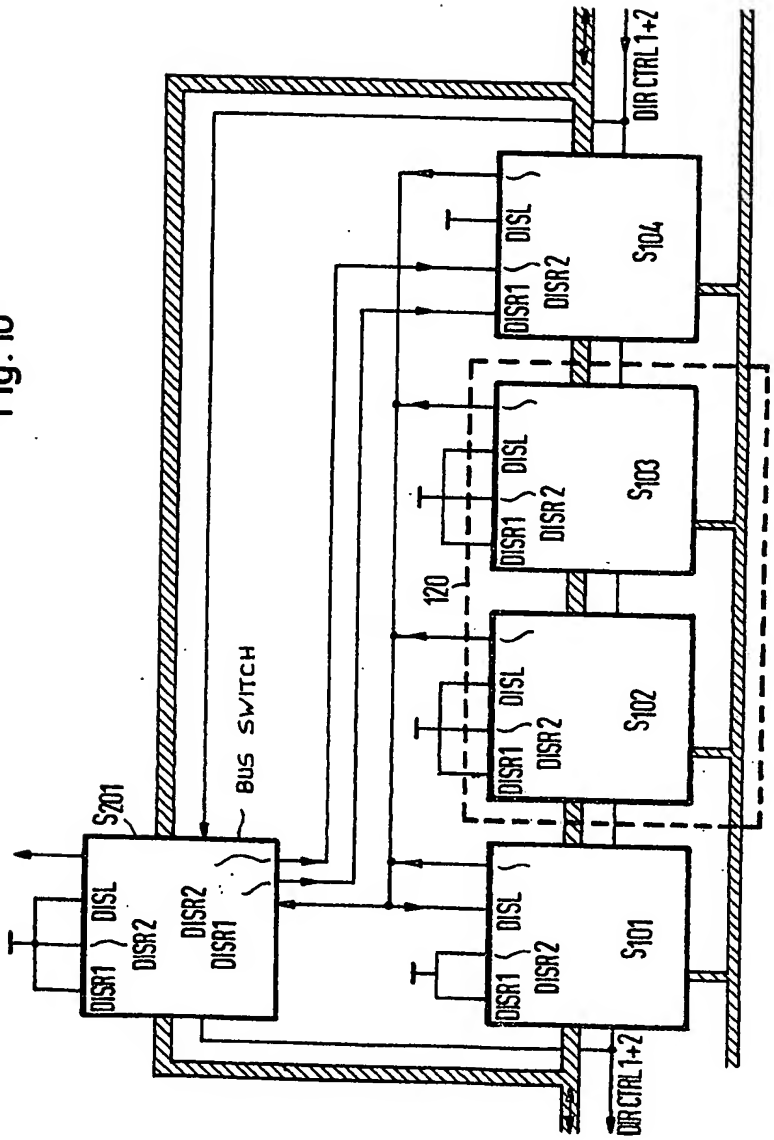

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Fig. 11

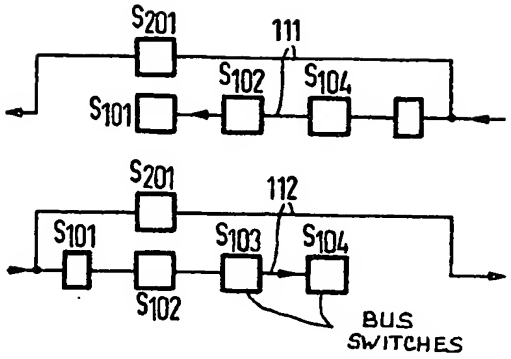

Fig. 12

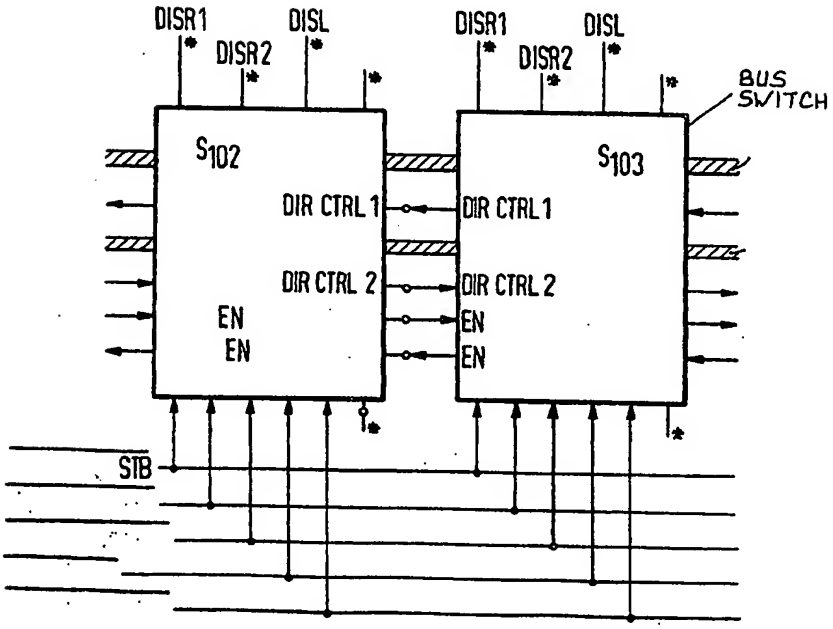

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Fig. 13

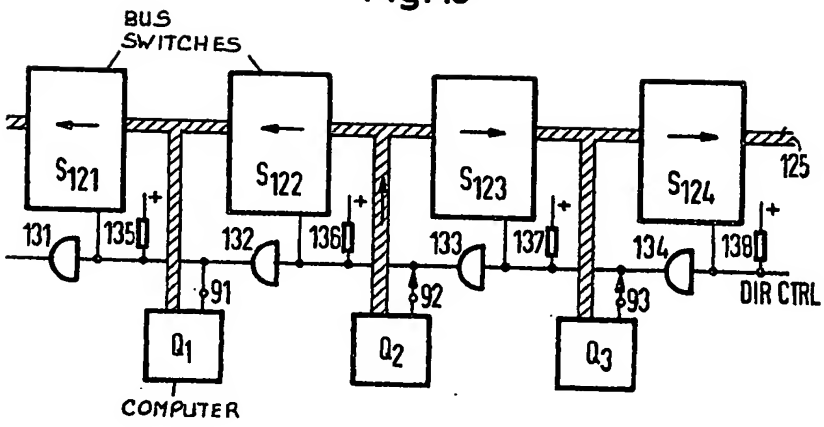
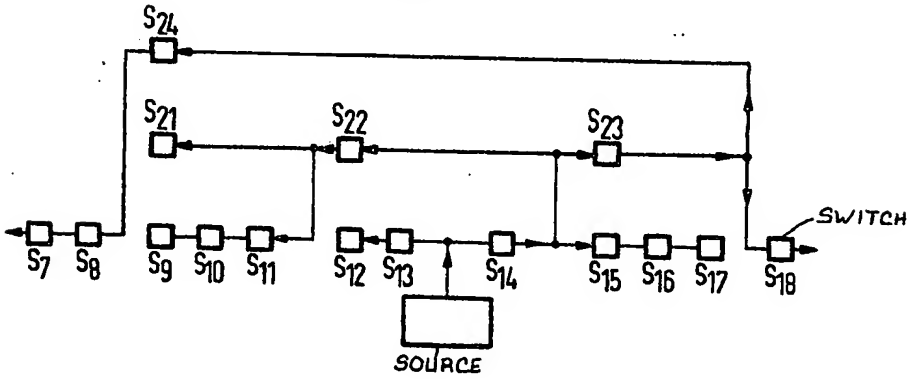


Fig. 14



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